Specification

OSFP RHS 400G SR4 Transceiver

(Preliminary)

T E S – L 1 6 H 9 – 8 C Z

Ordering Information

Model Name	TES-L16H9-8CZ	Note
Voltage	3.3V	
Device type	850nm VCSEL	
Temperature	0°C~+70°C	
Distance	60m (OM3) / 100m (OM4)	
Optical interface	MPO-12 connector	
Latch Color	Beige	

Features

- 4x100G PAM4 retimed 400GAUI-4 electrical interface
- Single MPO- 12/APC optical connectors
- 4 channel VCSEL arras and 4 channels PIN photo detector arrays
- Maximum reach: 60m / 100m via OM3/ OM4 fiber
- Single 3.3V power supply
- Hot pluggable, RoHS compliant
- Compliant with CMIS 5.2
- Compliant to OSFP Module Specification Rev 5.0
- Compliant with IEEE 802.3db
- Complaint to IEEE 802.3ck
- Less than 9W in Case temperature range of 0 to +70°C

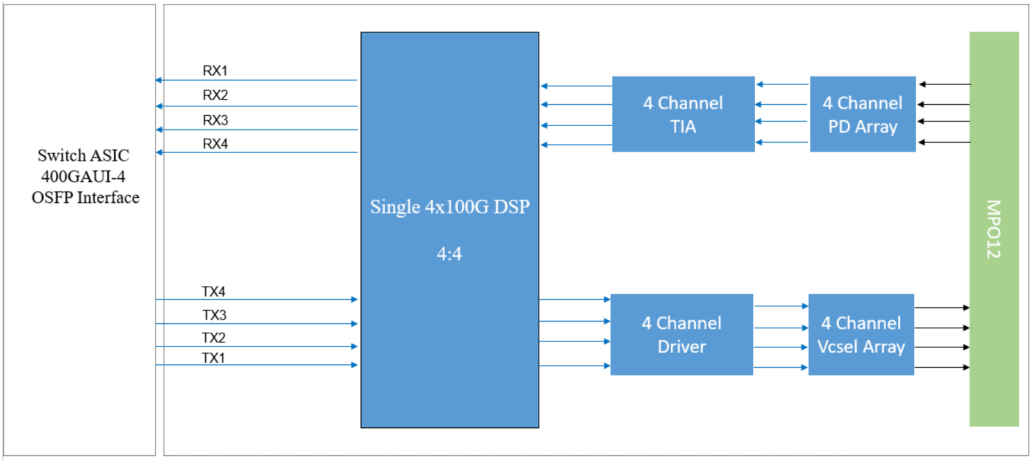
Applications

- 400GBASE-SR4 400G Ethernet
- 400G Infiniband NDR
- Data Center and Enterprise Networking

General Description

TES-L16H9-8CZ is a four-Channel, Parallel, Pluggable, Fiber-Optic OSFP for 400Gigabit Ethernet applications. This transceiver is a high performance module for short-range data communication and interconnect application. It integrates four data lanes in each direction with 4x53.125GBd. The length of OSFP SR4 is up to 60 meters over OM3 MMF or 100 meters over OM4 MMF. This module is designed to operate over multimode fiber systems using a nominal wavelength of 850nm.

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Maximum Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Ts	-40		85	℃	
Relative Humidity (no-condensation)	RH	15		85	%	
Operating Case Temperature	Top	0		70	℃	
Receiver Damage Threshold, per Lane	PRdmg	5			dBm	

Recommended Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Operating Case Temperature	Top	0		70	ºC	
Relative Humidity (non-condensing)	RH	15		85	%	
Power Supply Voltage	Vcc	3.135		3.465	V	
Total Power Consumption	Pc	-		9	W	1
Supply Current				2.87	A	
Bit Rate	BR			425	Gbps	
Fiber Length on OM3 MMF				60	m	
Fiber Length on OM4 MMF				100	m	
I2C Clock Frequency		0		1000	kHz	
Date Rate, each Lane		-	53.125	-	GBd	

Note:

1. Under condition of 3.465V operating supply voltage, and 70ºC case temperature.

Optical Characteristics

Parameter		Symbol	Min	Typ.	Max	Unit	Note
Transmitter							
Data rate per lane		DR		53.125		GBd	
Modulation format				PMA4			
Wavelength		λC	844	850	863	nm	1
RMS spectral width		σ			0.6	nm	
Average launch power, each lane		P_{AVG}	-1		4.0	dBm	
Optical Power OMA, each lane, max		P_{OMA}		3.5		dBm	
OMAouter, each lane min	Max (TECQ, TDECQ) <1.8 dB		max [-2.6, max (TECQ, TECQ) -4.4]			dBm	
	1.8 < max (TECQ, TDECQ) < 4.4 dB						
Transmitter and Dispersion eye closure, each lane		TDECQ			4.4	dB	
Transmitter eye closure for PMA4 (TECQ), each lane		TECQ			4.4	dBm	
Extinction Ratio			2.5			dB	
Transmitter power excursion, each lane					2.3	dBm	
Optical Return Loss Tolerance		ORLT			14	dB	
Optical Power for TX DISABLE					-30	dBm	
Encircled fluxb			≥86% at 19 um			dBm	
			≤30% at 4.5 um			dB	

Notes:

1. Defined according to the performance of the laser used.
2. Measured into type A1a.2 or type A1a.3, or A1a.4, 50 um fiber, in accordance with IEC 61280-1-4

Parameter		Symbol	Min	Typ.	Max	Unit	Note
Receiver							
Data rate per lane		BR		53.125		Gbd	
Modulation format				PAM4			
Lane Wavelength		λ	842	850	863	nm	
Damage Threshold, average optical power, each lane			5	-	-	dBm	
Average receive power, each lane			-6.4	-	4.0	dBm	
Receive Power (OMA_{outer}), each lane			-	-	3.5	dBm	
Receiver Reflectance		Rr	-	-	-15	dB	
Receiver sensitivity (OMA), each lane			RS = max (-4.6, TECQ – 6.4)			dBm	1
Stressed receiver sensitivity, each lane					-2	dBm	
Rx Los	Assert		-15			dBm	
	De-assert				-7.5	dBm	
	Hysteresis		0.5		5	dB	

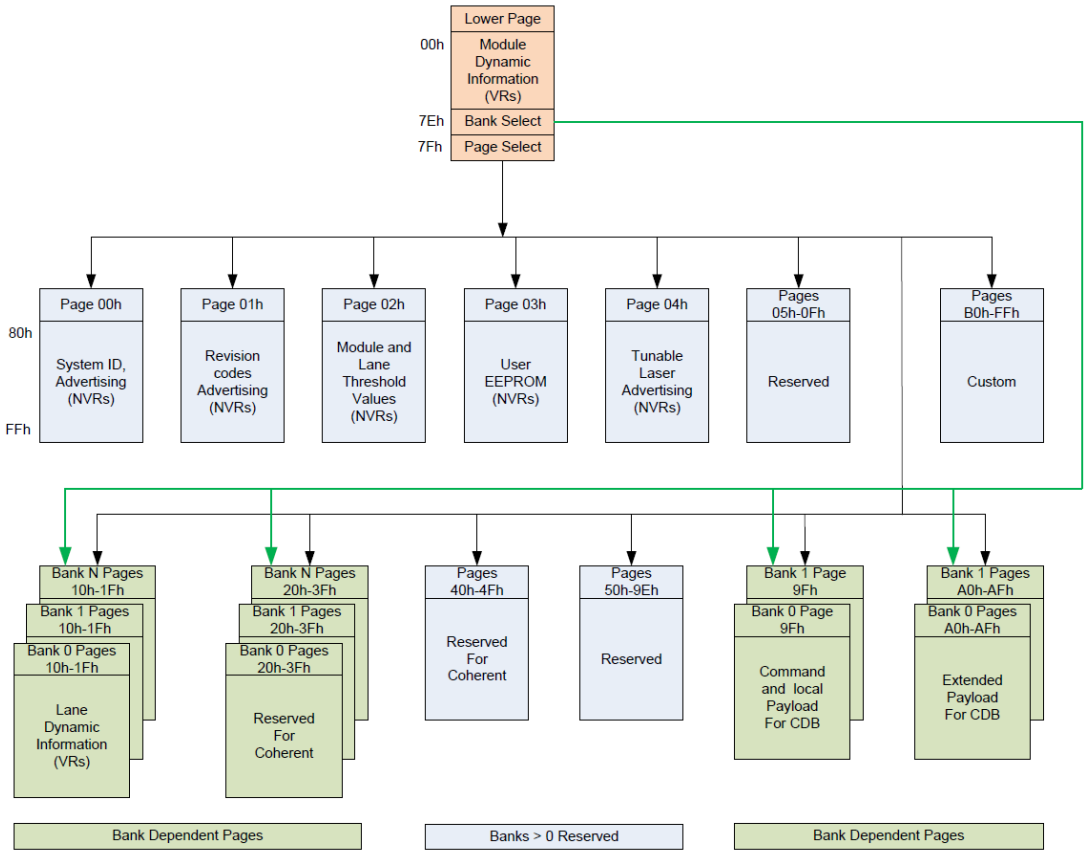
Notes:

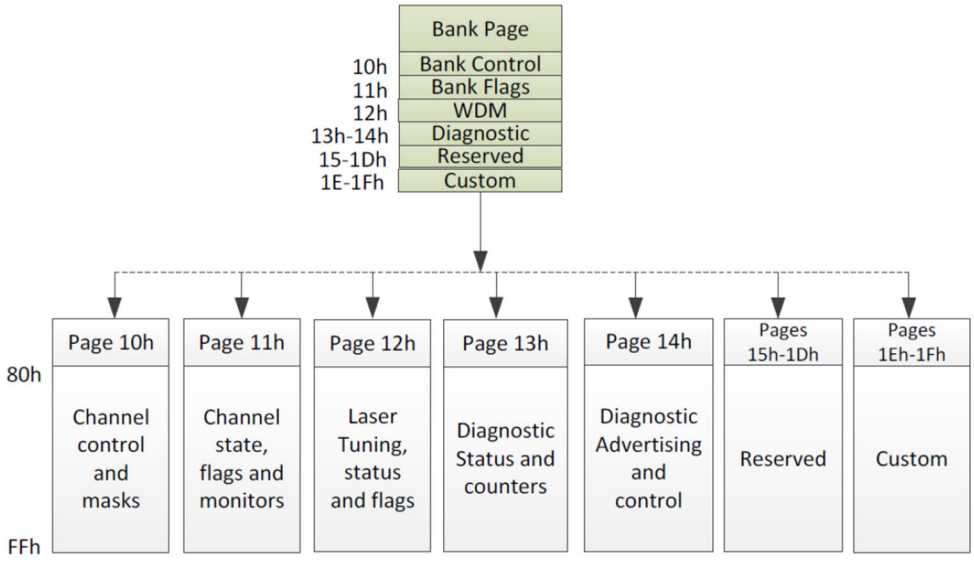
1. Receiver sensitivity is informative and is defined for a transmitter with a value of TECQ. Measured with conformance test signal at TP3 for BER = 2.4E-4 Pre-FEC.

Electrical Characteristics

Parameter	Min	Typ.	Max	Unit	Note
Pre FEC Bit Error Ratio			2.4E-4		
Post FEC Bit Error Ratio			1E-12		
Transmitter (each Lane)					
Differential pk-pk Input Voltage tolerance	750			mV	
Differential Termination Mismatch			10	%	
Eye hfour	10			mV	
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)			dB	
Vertical eye closure			12	dB	
Effective return loss	7.3			dB	
Transition Time	10			ps	
Receiver (each Lane)					
Differential data output swing	300		900	mVpp	
Differential termination mismatch			10	%	
Eye hfour	15			mV	
Vertical eye closure			12	dB	
Common-mode to differential-mode return loss	IEEE802.3ck Equation (120G–1)				
Effective return loss	8.5			dB	
Transition time	8.5			ps	

Memory Map


Lower Page
00h
Module Dynamic Information (VRs)
7Eh
Bank Select
7Fh
Page Select
Page 00h
80h
System ID, Advertising (NVRs)
FFh
Page 01h
Revision codes Advertising (NVRs)
Page 02h
Module and Lane Threshold Values (NVRs)
Page 03h
User EEPROM (NVRs)
Page 04h
Tunable Laser Advertising (NVRs)
Pages 05h-0Fh
Reserved
Pages B0h-FFh
Custom
Bank N Pages 10h-1Fh
Bank 1 Pages 10h-1Fh
Bank 0 Pages 10h-1Fh
Lane Dynamic Information (VRs)
Bank N Pages 20h-3Fh
Bank 1 Pages 20h-3Fh
Bank 0 Pages 20h-3Fh
Reserved For Coherent
Pages 40h-4Fh
Reserved For Coherent
Pages 50h-9Eh
Reserved
Bank 1 Page 9Fh
Bank 0 Page 9Fh
Command and local Payload For CDB
Bank 1 Pages A0h-AFh
Bank 0 Pages A0h-AFh
Extended Payload For CDB
Bank Dependent Pages
Banks > 0 Reserved
Bank Dependent Pages


Bank Page
10h
Bank Control
11h
Bank Flags
12h
WDM
13h-14h
Diagnostic
15-1Dh
Reserved
1E-1Fh
Custom
Page 10h
80h
Channel control and masks
FFh
Page 11h
Channel state, flags and monitors
Page 12h
Laser Tuning, status and flags
Page 13h
Diagnostic Status and counters
Page 14h
Diagnostic Advertising and control
Pages 15h-1Dh
Reserved
Pages 1Eh-1Fh
Custom

Multiple Applications Support

The FHMD-85SRC supports CMIS 5.2 defined Application Advertising, Application Selection and Instantiation.

Application Advertising

Address (Dec)	Application		Value (Hex)	Description
	AppSel Code	Name		
85	NA	Module Type encoding	1	Optical Interfaces: MMF
86	0001b	HostInterfaceID	4B	HostInterfaceIDApp1:100GAUI-1-S C2M
87		MediaInterfaceID	D	MediaInterfaceIDApp1:100GBASE-SR
88		HostLaneCount&MediaLaneCount	11	LaneCountApp1： TX & RX 1 lanes
89		HostLaneAssignmentOptions	F	Permissible first host lane number: lanes 1, 2, 3, 4,
01h:176		MediaLaneAssignmentOptions	F	Permissible first media lane number: lanes 1, 2, 3, 4
90	0010b	HostInterfaceID	F	HostInterfaceIDApp2:200GAUI-4
91		MediaInterfaceID	E	MediaInterfaceIDApp2:200GBASE-SR4
92		HostLaneCount&MediaLaneCount	44	LaneCountApp2:TX & RX 4 lanes
93		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:177		MediaLaneAssignmentOptions	1	Permissible first media lane numbern: lane 1
94	0011b	HostInterfaceID	C	HostInterfaceIDApp3:100GAUI-4 C2M
95		MediaInterfaceID	0	MediaInterfaceIDApp3: SFF-8024 Undefined
96		HostLaneCount&MediaLaneCount	44	LaneCountApp3:TX & RX 4 lanes
97		HostLaneAssignmentOptions	1	Permissible first host lane number: lane 1
01h:178		MediaLaneAssignmentOptions	1	Permissible first media lane number: lane 1
98	0100b	HostInterfaceID	4F	HostInterfaceIDApp4:400G S C2M
99		MediaInterfaceID	11	MediaInterfaceIDApp4:400G-SR4
100		HostLaneCount&MediaLaneCount	44	LaneCountApp4:TX & RX 4 lanes
101		HostLaneAssignmentOptions	1	HostLaneAssignmentOptionsApp4:begin lane 1

01h:179		MediaLaneAssignment Options	1	Permissible first media lane number: lane 1
102	0101b	HostInterfaceID	4D	HostInterfaceIDApp5:200GAUI-2-S C2M
103		MediaInterfaceID	1B	MediaInterfaceIDApp5:200GBASE-SR2
104		HostLaneCount&Media LaneCount	22	LaneCountApp5： TX & RX 2 lanes
105		HostLaneAssignmentO ptions	5	Permissible first host lane number: lanes 1, 3,
01h:180		MediaLaneAssignment Options	5	Permissible first media lane number: lanes 1, 3
106			FF	HostInterfaceIDApp6
107			0	MediaInterfaceIDApp6
108			0	LaneCountApp6
109			0	HostLaneAssignmentOptionsApp6
110			0	HostInterfaceIDApp7
111			0	MediaInterfaceIDApp7
112			0	LaneCountApp7
113			0	HostLaneAssignmentOptionsApp7

As shown in the table above, the TES-K16H9-8CZ supports 5 applications, 400GBASE-SR4, 200GBASE-SR4, 100GBASE-SR4, 2X200GBASE-SR2, 4X100GBASE-SR1

Application Selection and Instantiation

The host can select Applications by programming the AppSel value in Staged Set 0. AppSel=1 is the default Application populated in the Active Control Set at power-on or reset.

**Note that the channels of the module are independent and can be configured separately.(ie. up to four 100GBASE-SR instances can be configured), however, it does not support different applications with different channels at the same time*

TES-K16H9-8CZ supports two methods of application selection and instantiation. The first method is implemented according to CMIS, and the second method is customized, which is simpler.

- **First method:**

The applications switching configuration sequence is as follows: read Application Descriptor Registers and select the required Appsel. Write application configuration to DPConfigLane<i> in Stage Control Set 0, then write 1 to ApplyDPInitLane<i> to trigger Application Instantiation. The Active Set can be read from page11h.

For example, select AppDescriptor3:

Step 1: Write 0x30 in Page10h Byte145~Byte152(8 bytes)—Set AppselCode3

Step 2: Write 0xFF in Page10h Byte143—Set trigger register to run Application Instantiation.

- **Second method:**

Set the value of Page10h Byte240. This is a private definition.

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	100GBASE-SR1
1	00000001b	200GAUI-4	200GBASE-SR4
2	00000010b	100GAUI-4	100GBASE-SR4
3	00000011b	400GAUI-4-S C2M	400GBASE-SR4
4	00000100b	200GAUI-2-S C2M	200GBASE-SR2

TX & RX Squelch

Default TX and RX auto-squelch is enabled. But TX and RX auto squelch disable, and force squelching function are not supported.

TX input Equalization

Default TX adaptive equalization is enabled. But TX adaptive equalization disable, and fixed equalization adjust function are not supported.

RX output Equalization

RX output Equalization follows CMIS Table as below, with default 1dB, readable and writable.

Rx Output Equalization Codes

Code Value	Bit pattern	Post-Cursor Equalization	Pre-Cursor Equalization
0	0000b	0dB (No Equalization)	0dB (No Equalization)
1	0001b	1 dB	0.5 dB
2	0010b	2 dB	1.0 dB
3	0011b	3 dB	1.5 dB
4	0100b	4 dB	2.0 dB
5	0101b	5 dB	2.5 dB
6	0110b	6 dB	3.0 dB
7	0111b	7 dB	3.5 dB
8-10	1000b-1010b	**Reserved**	**Reserved**
11-15	1011b-1111b	Custom	Custom

RX output amplitude

RX output amplitude follows CMIS Table 6-8, Rx output amplitude is the difference peak-to- peak EYE high when Rx output equalization is set to 0dB. The default value of output amplitude is set to 2, with typical differential 600mVp-p.

Table 6-8 Rx Output Amplitude Codes

Code Value	Bit pattern	Output Amplitude
0	0000b	100-400 mV (P-P)
1	0001b	300-600 mV (P-P)
2	0010b	400-800 mV (P-P)
3	0011b	600-1200 mV (P-P)
4-14	0100b-1110b	**Reserved**
15	1111b	Custom

Loopback capabilities

Media side input loopback and Host side input loopback feature are supported, loopback control method refers to CMIS.

Rx Output Equalization code table

Byte	Bits	Field Name	Field Description
13h:128	6	Simultaneous Host And Media Side loopbacks	0b: not supported
	5	Per Lane Media Side Loopbacks	1b: supported
	4	Per Lane Host Side Loopbacks	1b: supported
	3	Host Side Input Loopback	1b: supported
	2	Host Side Output Loopback	1b: supported
	1	Media Side Input Loopback	1b: supported
	0	Media Side Output Loopback	1b: supported

Digital Diagnostic Monitor Accuracy

The following characteristics are defined over recommended operating conditions.

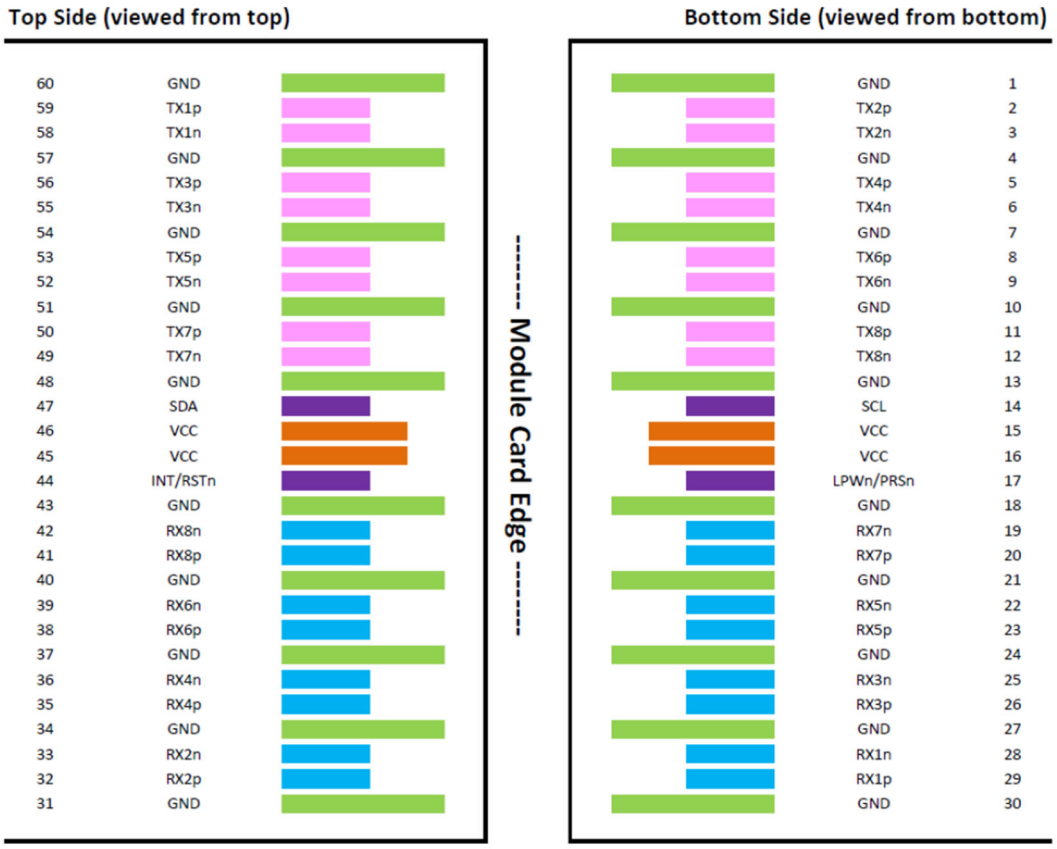
Digital Diagnostic Monitor Accuracy

Parameter	Accuracy	Unit
Internally measured transceiver temperature[1]	+/-3	°C
Internally measured transceiver supply voltage	+/-3	%
Measured Tx bias current	+/-10	%
Measured Tx output power[2]	+/-3	dB
Measured Rx received average optical power	+/-3	dB

Notes:

1. Test point is the hotspot of the module.
2. DDM reports stability within 0.5 dB when temperature is stable. TX DDM reports -40 dBm when TX disable.

Module Pad Assignments and Descriptions



Pin	Name	Logic	Description	Plug Sequence	Notes
1	GND		Ground	1	
2	Tx2p	CML-I	Receiver Data Non-Inverted	3	
3	Tx2n	CML-I	Receiver Data Inverted	3	
4	GND		Ground	1	
5	Tx4p	CML-I	Receiver Data Non-Inverted	3	
6	Tx4n	CML-I	Receiver Data Inverted	3	
7	GND		Ground	1	
8	Tx6p	CML-I	Receiver Data Non-Inverted	3	
9	Tx6n	CML-I	Receiver Data Inverted	3	
10	GND		Ground	1	

11	TX8p	CML-I	Receiver Data Non-Inverted	3	
12	TX8n	CML-I	Receiver Data Inverted	3	
13	GND		Ground	1	
14	SCL	LVCMOS-I/O	2-wire Serial interface clock	3	
15	VCC		+3.3V Power	2	
16	VCC		+3.3V Power	2	
17	LPWn/PRSn	Multi-Level	Low-Power Mode / ModulePresent	3	1A
18	GND		Ground	1	
19	RX7n	CML-O	Receiver Data Inverted	3	
20	RX7p	CML-O	Receiver Data Non-Inverted	3	
21	GND		Ground	1	
22	RX5n	CML-O	Receiver Data Inverted	3	
23	RX5p	CML-O	Receiver Data Non-Inverted	3	
24	GND		Ground	1	
25	RX3n	CML-O	Receiver Data Inverted	3	
26	RX3p	CML-O	Receiver Data Non-Inverted	3	
27	GND		Ground	1	
28	RX1n	CML-O	Receiver Data Inverted	3	
29	RX1p	CML-O	Receiver Data Non-Inverted	3	
30	GND		Ground	1	
31	GND		Ground	1	
32	RX2p	CML-O	Receiver Data Non-Inverted	3	
33	RX2n	CML-O	Receiver Data Inverted	3	
34	GND		Ground	1	
35	RX4p	CML-O	Receiver Data Non-Inverted	3	
36	RX4n	CML-O	Receiver Data Inverted	3	
37	GND		Ground	1	
38	RX6p	CML-O	Receiver Data Non-Inverted	3	
39	RX6n	CML-O	Receiver Data Inverted	3	
40	GND		Ground	1	

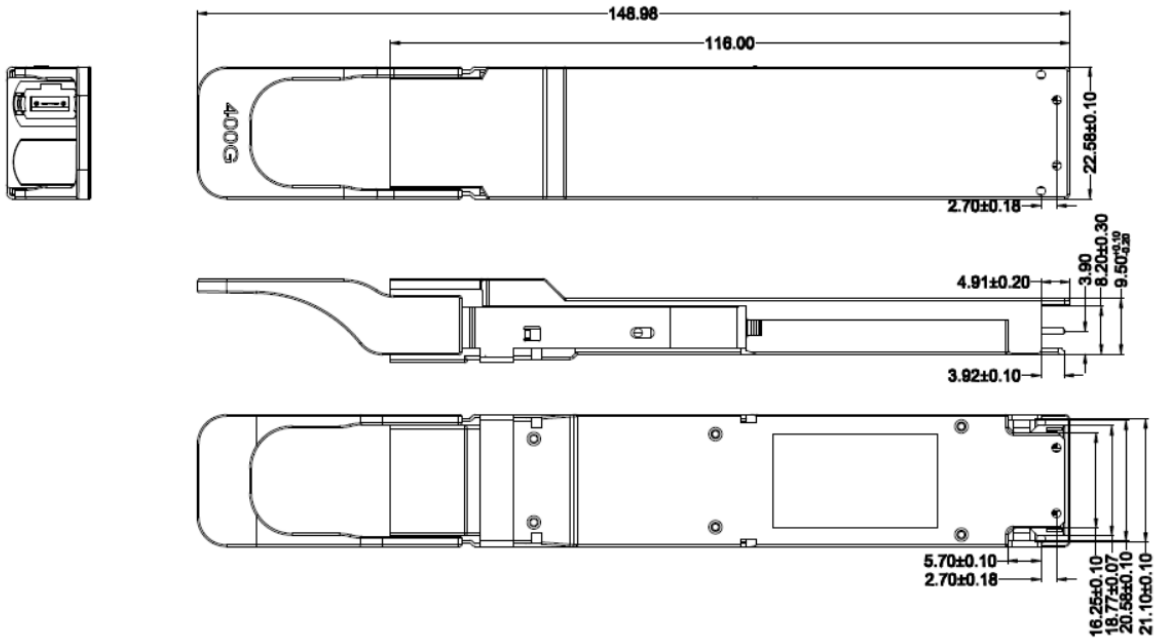
41	RX8p	CML-O	Receiver Data Non-Inverted	3	
42	RX8n	CML-O	Receiver Data Inverted	3	
43	GND		Ground	1	
44	INT/RSTn	Multi-Level	Module Interrupt / ModuleReset	3	1B
45	VCC		+3.3V Power	2	
46	VCC		+3.3V Power	2	
47	SDA	LVCMOS-I/O	2-wire Serial interface data	3	
48	GND		Ground	1	
49	TX7n	CML-I	Transmitter Data Inverted	3	
50	TX7p	CML-I	Transmitter Data Non-Inverted	3	
51	GND		Ground	1	
52	TX5n	CML-I	Transmitter Data Inverted	3	
53	TX5p	CML-I	Transmitter Data Non-Inverted	3	
54	GND		Ground	1	
55	TX3n	CML-I	Transmitter Data Inverted	3	
56	TX3p	CML-I	Transmitter Data Non-Inverted	3	
57	GND		Ground	1	
58	TX1n	CML-I	Transmitter Data Inverted	3	
59	TX1p	CML-I	Transmitter Data Non-Inverted	3	
60	GND		Ground	1	

Notes:

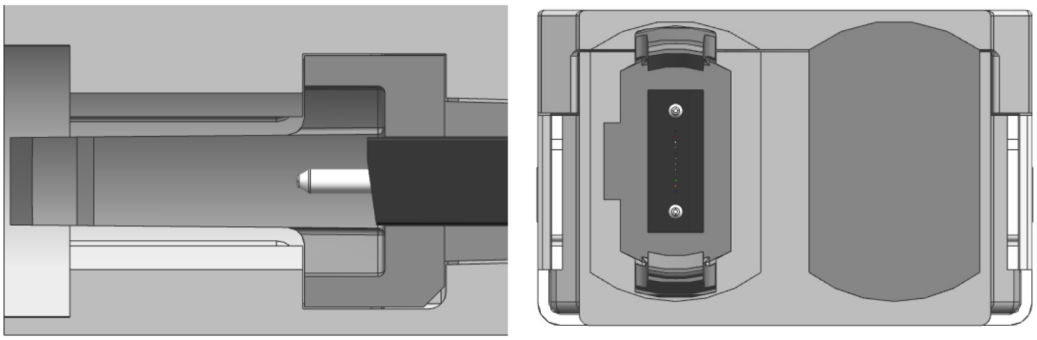
1. Plug Sequence specifies the mating sequence of the host connector and module. The contact sequence is 1, 2, 3
2. LPWn/PRSn is a Multi-level signal for low power control from host to module and module presence indication from module to host. It designed according to OSFP Module Specification Section 13.5.3
3. INT/RSTn is a Multi-level signal for interrupt request from module to host and reset control from host to module. It designed according to OSFP Module Specification Section 13.5.2

Mechanical Design Diagram

Unit: mm



Optical Interface



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Revision History

Date	Version	Description
3/21/2024	0.1	Preliminary release
5/21/2024	0.2	Modified P/N to meet coding rule
6/21/2024	0.3	Updated specification